PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Leonard Forbes et al.	)	Examiner: George Eckert II
	)	
Serial No.: 08/903453	)	Group Art Unit: 2815
	)	
Filed: July 29, 1997	)	Docket: 303.378US1
	)	
For: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS	)	

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on October 15, 2003, from the Final Rejection of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 of the above-identified application, as set forth in the Final Office Action mailed on July 15, 2003.

This Appeal Brief is filed in triplicate. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 330.00 which represents the requisite fee set forth in 37 C.F.R. § 117. The Appellants respectfully request consideration and reversal of the Examiner's rejections of the pending claims 2, 3, 24-28, 41-48, 50-52, and 65-68.

APPELLANTS' BRIEF ON APPEAL

TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC, a Delaware corporation doing business at 8000 So. Federal Way, Boise, ID 83707, in an assignment recorded on July 30, 1997 (Reel/Frame 8654/0929-0935).

2. RELATED APPEALS AND INTERFERENCES

An Appeal Brief was filed on November 25, 2003 for U.S. Serial Number 09/134713, applicant Leonard Forbes et al., filed on August 14, 1998, and entitled DEAPROM Having Amorphous Silicon Carbide Gate Insulator.

3. STATUS OF THE CLAIMS

Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are pending in the application. Claims 1, 4-6, 20-23, 29-40, 49, and 53-64 have been canceled. Claims 7-19 have been withdrawn from consideration. Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are finally rejected.

4. STATUS OF AMENDMENTS

No Amendment has been filed by the applicant subsequent to the Final Office Action dated 15 July 2003.

5. SUMMARY OF THE INVENTION

A transistor according to an embodiment of the present invention is shown in Figure 1 of the application:

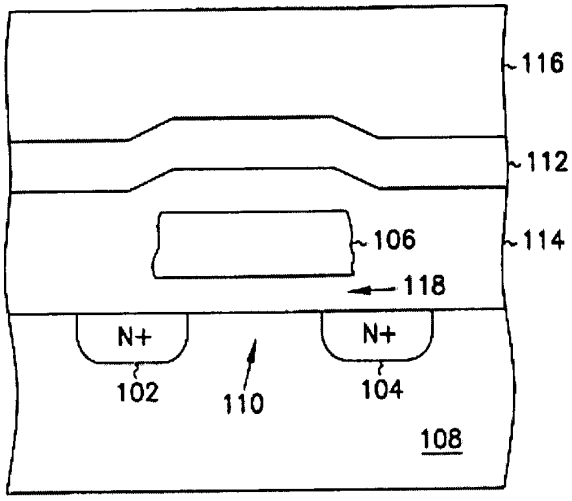


FIG. 1

A transistor according to an embodiment of the present invention comprises a source region 102 in a substrate 108, a drain region 104 in the substrate 108, a channel region 110 between the source region 102 and the drain region 104 in the substrate 108, and a gate 106 separated from the channel region 110 by a layer of amorphous carburized silicon 118 that was grown on the substrate 108. In other embodiments of the present invention, the gate 106 is a floating gate 106, and the transistor further comprises a control gate 112 separated from the floating gate 106 by a layer of insulating material 114.

6. ISSUES PRESENTED FOR REVIEW

I. Were claims 2, 3, 24-28, 41-48, 50-52 and 65-67 properly rejected under 35 USC §103 as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns)?

II. Were claims 2, 3, 24-28, 41, 45, 46, 50, and 65 properly rejected under 35 USC §103(a) as being unpatentable over Lott et al. (*Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, Lott-2) in view of Sakata et al. (Electronics

Letters, Vol. 30 No. 9, pp.688-689, Sakata)?

III. Were claims 42, 43, 47, 48, 51, 52, 66 and 67 properly rejected under 35 USC §103(a) as being unpatentable over Lott-2 in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns)?

IV. Was claim 68 properly rejected under 35 USC §103 as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns), or as being unpatentable over Lott et al. (*Charge Storage in InAIAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, Lott-2) in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata)?

7. GROUPING OF CLAIMS

Claims 2, 3, 24-28, 41, 45, 46, 50, and 65 stand together for purposes of this appeal.
Claims 42, 43, 47, 48, 51, 52, 66 and 67 stand together for purposes of this appeal.
Claim 44 stands alone for purposes of this appeal.
Claim 68 stands alone for purposes of this appeal.

Appellant does not make any admission that any claim may not be argued in another forum as independently patentable from any other claim. Additionally, Appellant's grouping of claims above is provided for the purposes of this Appeal Brief only.

8. ARGUMENT

The Applicable Law

All of the pending claims were rejected under 35 U.S.C. §103:

"A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a).

The MPEP states the following with regard to rejections under 35 USC § 103:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. " MPEP 2143.

A Federal Circuit opinion states that the suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art. *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). *See also* MPEP 2143.

The Federal Circuit has emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee*:

"When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness.....The factual inquiry whether to combine references must be thorough and searching....It must be based on objective evidence of record." *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

The Federal Circuit stated that the "need for specificity pervades this authority" requiring a teaching, motivation, or suggestion to select and combine references. *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). The Federal Circuit has expressed this need for specificity in several cases:

"[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.....the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

"[E]ven when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination." *In re Rouffet,* 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).

> "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." *In re Kotzab,* 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

Finally, the proposed modification in a rejection cannot change the principle of operation of the prior art being modified:

> "We hold, further, that the combination of Jepson with Chinnery et al. is not a proper ground for rejection of the claims here on appeal. This suggested combination of references would require a substantial reconstruction and redesign of the elements shown in Chinnery et al. as well as a change in the basic principles under which the Chinnery et al. construction was designed to operate." *In re Ratti,* 123 USPQ 349, 352 (CCPA 1959). *See also* MPEP 2143.01.

Rejections

I. The Rejection of claims 2, 3, 24-28, 41-48, 50-52 and 65-67 under 35 U.S.C. §103.

Claims 2, 3, 24-28, 41-48, 50-52 and 65-67 were rejected under 35 U.S.C. §103 as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). Claims 2, 3, 24-28, 41, 45, 46, 50, and 65 stand together for purposes of this appeal. Claims 42, 43, 47, 48, 51, 52, 66 and 67 stand together for purposes of this appeal. Claim 44 stands alone for purposes of this appeal as the only claim rejected solely on these grounds. The appellant respectfully submits that the Office Action has not presented evidence of a reasonable expectation of success of this combination of Sakata and Sugita as required by *In re Vaeck* and *In re Lee.* The appellant also respectfully submits that there is no suggestion or motivation to form a device by combining elements from these references, and that Sakata in fact teaches away from this combination.

Representative of these claims, claim 46 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 a heterojunction (HJ) diode structure:

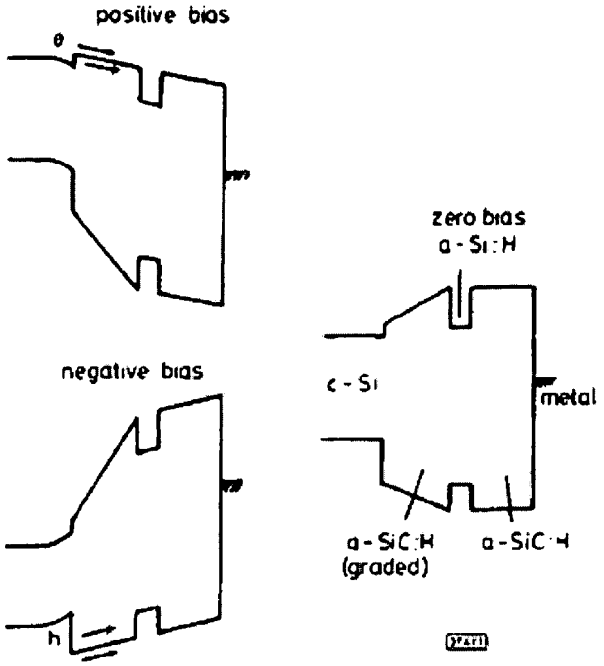


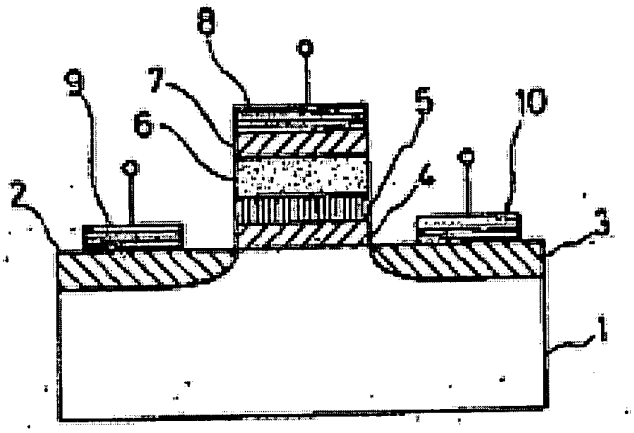
Fig. 1 *Schematic band diagrams of proposed a-SiC:H/a-Si:H heterojunction structure*

e and *h* denote electrons and holes, respectively

Sakata Figure 1.

The heterojunction (HJ) diode structure of Sakata includes c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, Column 3. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 46.

Sugita shows in Figure 1 a floating gate transistor with a source 2 and a drain 3 in a substrate 1, and a polysilicon floating gate 6 separated from the substrate 1 by an insulator 4, 5:



Sugita Figure 1.

As an initial matter, the final Office Action has not presented evidence of a reasonable expectation of success of this combination of Sakata, Sugita, and Burns as required by *In re Vaeck* and *In re Lee*. The Office Action has not established a *prima facie* case of obviousness without this element.

In addition, there is no suggestion or motivation to form a device by combining elements from Sakata, Sugita, and Burns. There are substantial differences between the principles of operation of the HJ diode structure of Sakata and the principles of operation of the floating gate transistor of Sugita. The HJ diode structure of Sakata is also referred to as "stacked insulator layers" through which both electrons and holes conduct. The principles of operation of the HJ diode structure of Sakata are described as follows:

> "With the application of positive (negative) bias to the metal gate, electrons (holes) are efficiently injected from the crystalline Si (c-Si) substrate into the thin a-Si:H layer through the compositionally graded a-SiC:H layer. When the bias voltage is restored to zero, injected electrons (holes) can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces.

By applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons (holes) and thus the memory is erased." Sakata, columns 1 and 2.

The known principles of operation of a floating gate transistor such as Sugita are substantially different. Burns describes the programming of a floating gate transistor with the language: "[e]lectrons are accelerated, ...and acquire enough energy to enter the conduction band of the gate oxide layer. There they are attracted by the positive potential on the select gate, and many of them lodge on the floating gate....When the programming voltage is removed, the electrons on the floating gate are trapped, and thus the floating gate constitutes a negative charge between the select gate and the substrate." Burns, page 383. Burns then describes the erasure of the floating gate transistor with UV light: "[t]he UV light imparts photon energy to the electrons, allowing them to escape through the oxide layer." Burns, page 383. Unlike the operation of the HJ diode structure of Sakata, only electrons are involved in programming and erasing a floating gate transistor according to Burns.

Forming a device by adding elements from Sugita to the HJ diode structure of Sakata would require a change in the basic principles under which the Sakata construction was designed to operate according to the quotes above, and therefore the teachings of Sakata and Sugita are not sufficient to render claim 46 *prima facie* obvious under *In re Ratti*. The final Office Action has not provided evidence showing that the basic principles of operation of Sakata would not be changed by the combination. In view of the differences between the principles of operation of Sakata and Sugita, one skilled in the art would need to see such evidence to find a suggestion for their combination.

Some statements in Sakata indicate that the HJ diode structure might be used in a memory device. For example, Sakata states that "the present structure can be used as a component of dynamic random access memories (DRAMs) [4] at room temperature." Sakata, page 689, column 1.

The applicant has submitted a paper entitled *Multi-Day Dynamic Storage of Holes at the AlAs/GaAs Interface* by Qian et al. (Qian). Qian shows a p+GaAs/AlAs/n-GaAs capacitor

structure in Figure 1 and uses a capacitance-voltage (CV) technique to measure the storage time of holes. Qian, Abstract and Figure 2. In the conclusion Qian notes the CV behavior of the capacitor structure and claims that it is appropriate for use in a dynamic RAM memory device.

The applicant notes that Sakata emphasizes the CV characteristics of Sakata's sample diode on page 688, column 2, and in particular Figure 2:

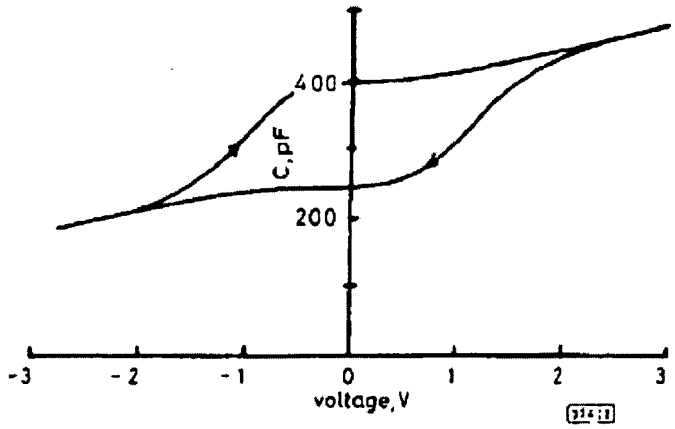


Fig. 2 *Capacitance-voltage characteristics of sample diode fabricated on n-type substrate with structure shown in Fig. 1*

Arrows in figure denote directions of bias sweep
f = 100kHz, dark, 0.4V/s

Sakata Figure 2.

The applicant respectfully submits that Sakata is suggesting in the text quoted above that the heterojunction structure can be used as a storage element in a DRAM device.

Sakata also states that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. The applicant respectfully submits that this statement does not comprise a clear and particular teaching or motivation to one skilled in the art at the time the invention was made to form a device by combining elements from Sakata, Sugita, and Burns, and in fact the whole of the text of Sakata teaches away from such a combination.

Sakata refers to a paper by Capasso et al. (Capasso, of record) with the sentence "Capasso *et al.* [2] reported similar memory devices based on AlGaAs/GaAs HJ." Sakata, page 688, column 2. Sakata is referring to the earlier statement in the same paragraph, quoted above,

that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Capasso reports AlGaAs/GaAs floating-gate memory devices. Capasso, abstract. Capasso does not show a picture of the device, but Capasso does comment on its operation:

> "Compared with conventional Si-based floating-gate devices this structure operates on a different injection method. Electrons are injected from the control gate into the floating gate using an AlGaAs graded-gap barrier." Capasso, Abstract. *See also* Capasso, column 1.

This is a substantially different principle of operation than that of a traditional floating gate transistor such as shown by Sugita and described above with reference to Burns. The translation of Sugita describes tunnel conduction at the interface between the silicon substrate 1 and the SiC film 5 in paragraphs [0019] and [0020]. Sugita also describes electrons stored in the cell 22 escape to the source and drain side by Fowler-Nordheim type tunnel injection in paragraph [0040]. The source 2 and drain 3 are shown in the silicon substrate 1 of Sugita.

Sakata indicates to one skilled in the art that a floating gate device with its heterojunction operates like Capasso's memory device that injects electrons from the control gate into the floating gate. The formation of a device from elements of Sakata, Sugita, and Burns would change the basic principles under which the Sakata construction was designed to operate according to Sakata and Capasso. This is further illustrated with the paper entitled *Anisotropic Thermionic Emission of Electrons Contained in GaAs/AlAs Floating Gate Device Structures* by Lott et al. (Lott-1) submitted by the applicant.

Lott-1 shows in Figure 1 the mask set and epitaxial layers of a floating gate transistor:

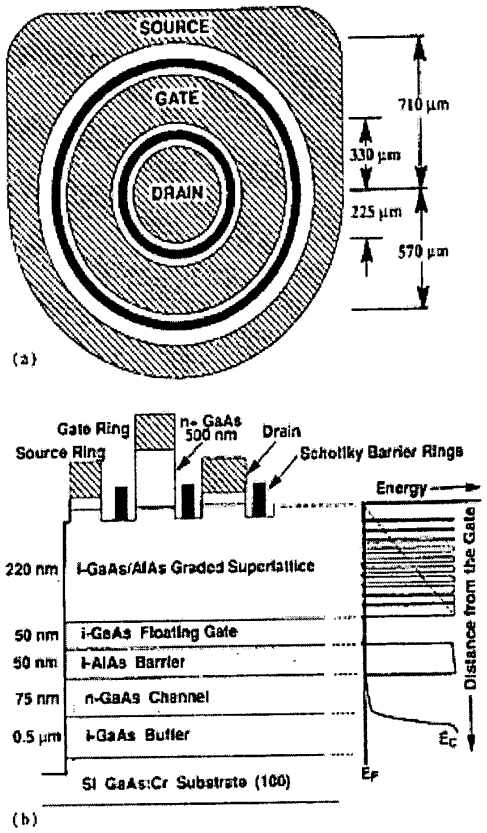


FIG. 1. Schematic is shown for (a) the mask set and (b) the epitaxial layers that make up the closed transistor used in this study. One half of the device structure is shown. A simplified first-order conduction-band diagram is shown alongside the device.

Lott-1 Figure 1.

Lott-1 refers to the transistor as "[o]ur test vehicle (Fig. 1) has a vertical structure similar to that of Capasso *et al.* " Lott-1 is referring here to the same Capasso paper that Sakata refers to in the quote above from page 688, column 2. The transistor structure shown in Figure 1 of Lott-1 is linked by Sakata and Lott-1 through Capasso to Sakata's earlier statement that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. This is a specific suggestion from Sakata to one skilled in the art about the use of its heterojunction in floating-gate memory devices. The transistor of Lott-1 has a source, a drain, a gate, and a floating gate. However, the source, drain, and gate shown in Lott-1 are formed next

to each other on a superlattice, and the floating gate of Lott-1 is on the other side of the superlattice. A barrier separates the floating gate of Lott-1 from the channel of Lott-1. The floating gate of Lott-1 is between the source and drain on one side and the channel on the other side, and separates the source and the drain from the channel.

The transistor structure of Lott-1 is substantially different from that of Sugita and Burns, even though both have elements with the names source, drain, and floating gate. Sakata is referring to the structure in Lott-1 when Sakata says that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. Sakata and Figure 1 of Lott-1 are linked by their reference to the same paper by Capasso. Lott-1 specifically says that the structure of Figure 1 is similar to that of Capasso. Sakata specifically says that Capasso reported similar memory devices.

The connection between the transistor of Lott-1 and Sakata is documented by a reference in both to Capasso. This is evidence of a suggestion to one skilled in the art to use the heterojunction of Sakata in a transistor such that in Lott-1. The structures of Lott-1 and Sugita and Burns are substantially different, and there is no comparable suggestion in the prior art to form a device by combining elements from Sakata, Sugita, and Burns.

The final Office Action states that the motivation for combining Sakata, Sugita, and Burns is that "the source, drain, and channel regions allow individual floating gate devices to be formed in an array....[t]he use of the source/drain/channel regions for such programming is well known in the art." Final Office Action, page 5. The office action did not cite evidence in the record, such as one of the references, that supports the above-stated motivation for combining Sakata, Sugita, and Burns as is required by *In re Lee*. The Office Action did not cite evidence showing that the HJ structure of Sakata must have a source and a drain in a substrate to be formed in an array.

The final Office Action states that "it is considered obvious to form the control gate of Sakata et al. from polysilicon." Final Office Action, page 6. The motivation making this substitution is stated above: "[t]here are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps." Final Office Action,

page 6. The final Office Action has not identified objective evidence in the record to support this motivation to modify Sakata as is required by *In re Lee.*

The applicant respectfully submits that the rejection of claims 2, 3, 24-28, 41-48, 50-52 and 65-67 under section 103 is improperly based on hindsight. The final Office Action has not addressed the clear textual links between Sakata, Capasso, and Lott-1 discussed above that are evidence of a suggestion to one skilled in the art to use the heterojunction of Sakata in a transistor such as that in Lott-1. The final Office Action has not supplied a comparable clear and particular teaching or motivation to combine Sakata, Sugita, and Burns as is required by *In re Dembiczak.* The final Office Action has not provided objective evidence from the prior art that such a combination would have a reasonable expectation of success as is required by *In re Lee* and *In re Vaeck.* Forming a device by adding elements from Sugita and Burns to the HJ diode structure of Sakata would require a change in the basic principles under which the Sakata construction was designed to operate according to the quotes above, and therefore the teachings of Sakata, Sugita, and Burns are not sufficient to render claim 46 *prima facie* obvious under *In re Ratti.*

The applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 24-28, 41-48, 50-52 and 65-67 has not been established in the final Office Action. Reversal of the rejection of claims 2, 3, 24-28, 41-48, 50-52 and 65-67 under 35 U.S.C. § 103 is respectfully requested.

II. The Rejection of claims 2, 3, 24-28, 41, 45, 46, 50, and 65 under 35 U.S.C. §103.

Claims 2, 3, 24-28, 41, 45, 46, 50, and 65 were rejected under 35 USC § 103(a) as being unpatentable over Lott et al. (*Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, Lott-2) in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata). Claims 2, 3, 24-28, 41, 45, 46, 50, and 65 stand together for purposes of this appeal. The appellant respectfully submits that the Office Action has not presented evidence of a reasonable expectation of success of this combination of Sakata and Sugita as required by *In re Vaeck* and *In re Lee.* The appellant also

respectfully submits that there is no suggestion or motivation to form a device by combining elements from these references.

Representative of these claims, claim 46 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 (reproduced above) a heterojunction (HJ) diode structure. The heterojunction (HJ) diode structure of Sakata includes c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, Column 3. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 46.

Lott-2 shows an InAIAs/InGaAs/InP floating gate heterostructure including a source, a drain, a floating gate, and a sense channel in Figure 1:

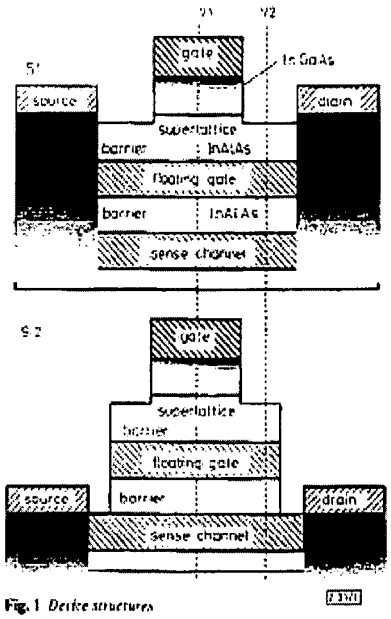


Fig. 1 *Device structures*

Lott-2 is also deficient as a reference in that, while Lott-2 shows the sense channel, it is a separate layer in the heterostructure of Lott-2, and is not shown as being part of the same

structure as the source and the drain of Lott-2. Therefore, even as combined, Sakata and Lott-2 do not show a channel region between a source region and a drain region in a substrate as is recited in claim 46.

There is also no suggestion or motivation to form a device by combining elements from Sakata and Lott-2. The final Office Action states the motivation for combining Lott-2 and Sakata is the statement in Sakata that "Capasso *et al.* [2] reported similar memory devices based on AlGaAs/GaAs HJ. However, excessive leakage current made it impossible to electrically erase the memories and a visible light pulse was instead used to erase the memory." Sakata, page 688, column 2.

This statement is not a specific suggestion to combine Lott-2 and Sakata. First of all, it refers to the specific device of Capasso, and not to III-V heterojunctions in general or the device in Lott-2. The final Office Action has not addressed the clear textual links between Sakata, Capasso, and Lott-1 discussed above that are evidence of a suggestion to one skilled in the art to use the heterojunction of Sakata in a transistor such as that in Lott-1. Second, the statement does not appear to be a suggestion to substitute parts of Sakata into the heterojunction of Capasso, but to replace it entirely. There is no indication in this statement that putting a silicon-based material into Capasso's heterojunction would solve the leakage problem. The final Office Action has not supplied a clear and particular teaching or motivation to combine Sakata and Lott-2 as is required by *In re Dembiczak.*

Additionally, the final Office Action is proposing to combine a silicon substrate c-Si and a silicon-based layer of Sakata with the InAlAs/InGaAs/InP heterostructure of Lott-2. More specifically, the final Office action proposes to replace the InAlAs barrier of Lott-2 with the hydrogenated amorphous silicon carbide a-SiC:H of Sakata. Final Office Action, page 9. The resulting structure would have silicon and non-silicon based layers in the same stack. The final Office Action has not provided objective evidence from the prior art that such a combination would have a reasonable expectation of success as is required by *In re Lee* and *In re Vaeck.*

Finally, forming a device by adding silicon-based layers from Sakata to the InAlAs/InGaAs/InP heterostructure of Lott-2 would require a change in the basic principles under which the Lott-2 construction was designed to operate in view of the different materials in

each stack, and therefore the teachings of Sakata and Lott-2 are not sufficient to render claim 46 *prima facie* obvious under *In re Ratti*. The final Office Action has not provided evidence showing that the basic principles of operation of Lott-2 would not be changed by the combination. In view of the differences in the materials of Sakata and Lott-2, one skilled in the art would need to see such evidence to find a suggestion for their combination.

The applicant respectfully submits that the rejection of claims 2, 3, 24-28, 41, 45, 46, 50, and 65 under section 103 is improperly based on hindsight. The final Office Action has not addressed the clear textual links between Sakata, Capasso, and Lott-1 discussed above that are evidence of a suggestion to one skilled in the art to use the heterojunction of Sakata in a transistor such as that in Lott-1. The final Office Action has not supplied a comparable clear and particular teaching or motivation to combine Sakata and Lott-2 as is required by *In re Dembiczak*. The final Office Action has not provided objective evidence from the prior art that such a combination would have a reasonable expectation of success as is required by *In re Lee* and *In re Vaeck*. Forming a device by adding silicon-based layers from Sakata to the InAIAs/InGaAs/InP heterostructure of Lott-2 would require a change in the basic principles under which the Lott-2 construction was designed to operate in view of the different materials in each stack, and therefore the teachings of Sakata and Lott-2 are not sufficient to render claim 46 *prima facie* obvious under *In re Ratti*.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 24-28, 41, 45, 46, 50, and 65 has not been established in the final Office Action. Reversal of the rejection of claims 2, 3, 24-28, 41, 45, 46, 50, and 65 under 35 U.S.C. § 103 is respectfully requested.

III. The Rejection of claims 42, 43, 47, 48, 51, 52, 66 and 67 under 35 U.S.C. §103.

Claims 42, 43, 47, 48, 51, 52, 66 and 67 were rejected under 35 USC § 103(a) as being unpatentable over Lott et al. (*Charge Storage in InAIAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, Lott-2) in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) and Burns et al.,

Principles of Electronic Circuits, pp. 382-383 (Burns). Claims 42, 43, 47, 48, 51, 52, 66 and 67 stand together for purposes of this appeal. The appellant respectfully traverses.

Representative of these claims, claim 47 recites the transistor of claim 46 (discussed above) wherein the substrate comprises a p-type silicon substrate, the source region comprises an n+-type source region in the substrate, the drain region comprises an n+-type drain region in the substrate, the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas, and further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

The Office Action states that it would have been obvious to form the device of Lott-2 and Sakata with the polysilicon control gate of Burns. "The motivation for doing so is that there are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps." Final Office Action, page 10.

The applicant respectfully submits that the rejection of claims 42, 43, 47, 48, 51, 52, 66 and 67 under section 103 is improperly based on hindsight. The final Office Action has not identified objective evidence in the record to support the above-stated motivation to combine Sakata, Lott-2, and Burns as is required by *In re Lee*. The final Office Action has not provided objective evidence from the prior art that such a combination would have a reasonable expectation of success as is required by *In re Lee* and *In re Vaeck*. Forming a device by adding silicon-based layers from Sakata and the polysilicon of Burns to the InAlAs/InGaAs/InP heterostructure of Lott-2 would require a change in the basic principles under which the Lott-2 construction was designed to operate in view of the different materials in each stack, and therefore the teachings of Sakata, Burns, and Lott-2 are not sufficient to render claim 47 *prima facie* obvious under *In re Ratti*.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 42, 43, 47, 48, 51, 52, 66 and 67 has not been established in the final Office Action. Reversal of the rejection of claims 42, 43, 47, 48, 51, 52, 66 and 67 under 35 U.S.C. § 103 is respectfully requested.

IV. The Rejection of claim 68 under 35 U.S.C. §103.

Claim 68 was rejected under 35 U.S.C. §103 as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). Claim 68 was also rejected under 35 USC § 103(a) as being unpatentable over Lott et al. (*Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, Lott-2) in view of Sakata.

Claim 68 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, a floating gate, and means for separating the floating gate from the channel region.

Claim 68 is a means-plus-function claim under 35 U.S.C. § 112, paragraph 6. MPEP 2181. Claim 68 stands alone for purposes of this appeal as the only means-plus-function claim pending in the application. The final Office Action has not provided an explanation or a rationale as to why the combinations of Sugita, Sakata, and Burns, or Lott-2 and Sakata show an equivalent to the corresponding elements disclosed in the specification. MPEP 2182, 2183.

The applicant respectfully submits that references as combined above do not show an equivalent to the corresponding elements disclosed in the specification under 35 U.S.C. § 112, paragraph 6. The applicant respectfully submits that a *prima facie* case of obviousness of claim 68 has not been established in the final Office Action. Reversal of the rejections of claim 68 under 35 U.S.C. § 103 is respectfully requested.

9. SUMMARY

For the foregoing reasons, the appellant respectfully submits that the rejections of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 under 35 U.S.C. § 103 were erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the rejected claims.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of December, 2003.

Amy Moriarty _____

Name Signature

APPENDIX

The Claims on Appeal

1. (Canceled)

2. (Original) An integrated circuit field effect transistor comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a gate supported by the substrate and extending between the source and drain above the channel; and

an insulative amorphous layer of carburized silicon grown on the channel and located between the channel and the gate.

3. (Previously Presented) An integrated circuit memory device supported by a semiconductor substrate, the device comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate supported by the substrate and extending between the source and drain above the channel;

a control gate formed adjacent to and insulated from the floating gate; and

an insulative layer of amorphous carburized silicon grown on the channel and located between the channel and the floating gate.

4 - 6. (Canceled)

7- 19. (Withdrawn)

20 - 23. (Canceled)

24. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate; and

a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

25. (Previously Presented) The transistor of claim 24 wherein the gate comprises a floating gate.

26. (Previously Presented) The transistor of claim 25, further comprising a control gate separated from the floating gate.

27. (Previously Presented) The transistor of claim 24 wherein the substrate comprises a semiconductor surface layer on an underlying insulating portion.

28. (Previously Presented) The transistor of claim 24 wherein the substrate comprises a doped silicon semiconductor substrate.

29 - 40. (Canceled)

41. (Previously Presented) The integrated circuit field effect transistor of claim 2 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region; and

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

42. (Previously Presented) The integrated circuit field effect transistor of claim 2 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region;

the gate comprises a floating gate isolated from the channel region by the amorphous layer of carburized silicon;

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

43. (Previously Presented) The device of claim 3 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region;

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

44. (Previously Presented) The transistor of claim 24 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

45. (Previously Presented) A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

46. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate; and

a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

47. (Previously Presented) The transistor of claim 46 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate;

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

48. (Previously Presented) A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region between the source region and the drain region in the substrate;

a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate; and

a polysilicon control gate separated from the floating gate by a layer of insulating material.

49. (Canceled)

50. (Previously Presented) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate;

a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region; and

a control gate separated from the floating gate.

51. (Previously Presented) The memory cell of claim 50 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate;

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

52. (Previously Presented) A memory cell comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate;

a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region; and

a polysilicon control gate separated from the floating gate by a layer of insulating material.

53 - 64. (Canceled)

65. (Previously Presented) The transistor of claim 45 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

66. (Previously Presented) The transistor of claim 48 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

67. (Previously Presented) The memory cell of claim 52 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

68. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate;

a floating gate; and

means for separating the floating gate from the channel region.